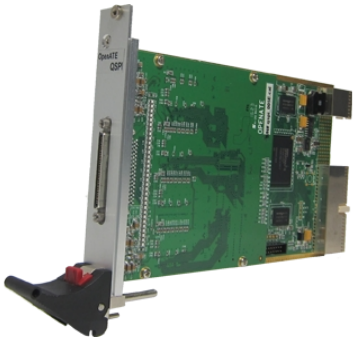
OpenATE QSPI

* Interface	3U PXI (V)	USB (V)
* 4 site x 8 input / output channels, IO dynamically configurable		
* 10 MHz data rate		
* -1V ~ +10V VOH VOL VIH VIL per channel		
* 32 PMU per board		
* 32 M of on-board vector memory per channel		
* 8 I2C Master to 400KHz CLK		
* 4 SPI Master to 10 MHz CLK		
* 1K failure log memory		
* 4 32 bit/ 10 ns counter/TMU		
* 4 gangable DPS 64~512mA		
* 4 CLK Generators 10MHz /10 ns		
* API & Pattern Editor		

3U PXI



USB

Description

The QSPI represents a multi-function of performance and capabilities for PXI-based digital instrumentation. The QSPI offers high performance pin electronics and 4 I2C masters and 4 32bit counter 4 clock generator in a compact, 3U PXI form factor. Each card can function as a quad sites I2C/SPI device tester, multiple cards can be interconnected, supporting up to 64 sites. The QSPI also supports deep pattern memory by offering 32M of on-board vector memory with dynamic per pin direction control and with test rates up to 10 MHz.

Features

The QSPI supports -1 ~ +10 VOH VOL VIH VIL per channel and 32 PMU per board. The QSPI offers 1 timing set, 2 driver TG Edges, 2 strobe TG Edges and four drive data formats are supported.
RTZ (Return To Zero), RTO (Return To One), NRZ (Non Return To Zero), SBC (Surround By Complement) which can provide flexibility to create a variety of bus cycles and waveforms to test board and box level products.

On-Board Memory

The QSPI offers 32 M of vector memory per site. Programmable pattern cycle times up to 2^{32} or infinite. There are pattern symbols including 0, 1, L, H, X, Z, J, Q.

Compatibility

All OpenATE Interfaces PXI cards comply with the PXI Specification 2.0 (issued Aug. 2000)

Software

The QSPI is supplied with API and Pattern Editor. Pattern Editor is a software tool that edits test patterns.

Application

- Automatic Test Equipment(ATE)
- Consumer Digital Functional Test
- Digital Pattern Generation
- I2C salve Device Testing

OpenATE QSPI

Specifications

● Pin Electronics	
I/O Channels	32, per board resource
Test rate	10MHz
Input Level (Vih/ Vil)	-1 ~ +10V per channel
Output Level (Voh/Vol)	-1 ~ +10V per channel
● Timing	
Period Resolution	10nS
Pin TG Edge Resolution	10nS
Minimum Pulse Width	50nS
Timing Sets	1
Driver TG Edges	2, per pin resource
Strobe TG Edges	2, per pin resource
● Formatter	
Format Sets	1
	RTZ, Return To Zero
	RTO, Return To One
	NRZ, Non Return To Zero
	NF, Non Format
	SBC, Surround By Complement
● PMU	
Number of PMU	32
PMU Accuracy	FI: 0.125%FS MI: 0.25%FS FV: 20mV MV :20mV
Number of IRange x 8	I1: ±2uA / I2: ±8uA
	I3: ±32uA / I4: ±128uA
	I5: ±512uA / I6: ±2mA
	I7: ±8mA / I8: ±32mA
Number of VRange x 1	E1: -1V ~ +10V
● Logic Sequencer	
Micro-Instructions	REPEAT; FC
Pattern Symbols	0, 1, L, H, X, Z, J, Q
LMSYNC to PXI Trigger Bus	For Sync with other Instruments
Ignore Fail By LM Address	YES
Vector Memory	32M(length) × 8(channels)
Programmable pattern cycle times	2^{32} or infinite
● I2C / SPI / Counter	
I2C master	8 / 400KHz
SPI master	4 / 10MHz
32 bits counter / TMU	4 / 10nS
● Trigger	PXI_TRIG Bus : 8

OpenATE QSPI

● Physical Properties	
Bus Interface	PXI
Dimensions	3U
Power Requirements	3.3V@3A, 5V@3A 12V@0.5A
System Clock	100MHz
Bus & Signals	8 PXI Trigger bus lines for parallel test
● Environmental	
Operating Temperature	0 ~ 50˚C
Storage Temperature	-20˚C ~ 70˚C
● Software	PXI : API & Pattern Editor USB: supplied with API Windows 10 only
● Maximum boards in one system	16
● PXI Compliance	All OpenATE Interfaces PXI cards comply with the PXI Specification 2.0 (issued Aug, 2000)

OpenATE Inc.

The Open Solution for IC Tester

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